IN THE CLAIMS

Please amend the claims as follows:

1-7. (Canceled)

8. (Currently Amended) ~~The method of claim 7~~ A method comprising:

translating a design description into a configuration for a plurality of heterogeneous processing elements in a heterogeneous reconfigurable device coupled to routers interconnected by a plurality of mesh interconnect networks, the plurality of mesh interconnect networks being allocatable to either data or control or a combination thereof; and

allocating the plurality of mesh interconnect networks between data and control, wherein allocating comprises determining whether latency constraints can be met with a shared data and control mesh network.

9. (Canceled)

10. (Currently Amended) ~~The method of claim 9 further comprising~~ A method comprising:

translating a design description into a configuration for a plurality of heterogeneous processing elements in a heterogeneous reconfigurable device coupled to routers interconnected by a plurality of mesh interconnect networks, the plurality of mesh interconnect networks being allocatable to either data or control or a combination thereof;

allocating the plurality of mesh interconnect networks between data and control, wherein translating and allocating results in a protocol file;

storing the protocol file in a memory; and

translating a second design description and performing a second allocation, resulting in a second protocol file, and storing the second protocol file in the memory.

11-30. (Canceled)

31. (New) The method of claim 8 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises dedicating the first plane to control and dedicating the second plane to data.

32. (New) The method of claim 8 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises allocating the first plane to be shared between data and control.

33. (New) The method of claim 8 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises allocating both the first plane and the second plane to be shared between data and control.

34. (New) The method of claim 8 wherein the plurality of heterogeneous processing elements are configurable to communicate over the plurality of mesh interconnect networks using packets of information.

35. (New) The method of claim 10 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises dedicating the first plane to control and dedicating the second plane to data.

36. (New) The method of claim 10 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises allocating the first plane to be shared between data and control.

37. (New) The method of claim 10 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises allocating both the first plane and the second plane to be shared between data and control.

38. (New) The method of claim 10 wherein the plurality of heterogeneous processing elements are configurable to communicate over the plurality of mesh interconnect networks using packets of information.

39. (New) An apparatus including a medium to hold machine-accessible instructions that when accessed result in a machine performing:

translating a design description into a configuration for a plurality of heterogeneous processing elements in a heterogeneous reconfigurable device coupled to routers interconnected by a plurality of mesh interconnect networks, the plurality of mesh interconnect networks being allocatable to either data or control or a combination thereof; and

allocating the plurality of mesh interconnect networks between data and control, wherein allocating comprises determining whether latency constraints can be met with a shared data and control mesh network.

40. (New) The apparatus of claim 39 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises dedicating the first plane to control and dedicating the second plane to data.

41. (New) The apparatus of claim 39 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises allocating the first plane to be shared between data and control.

42. (New) The apparatus of claim 39 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises allocating both the first plane and the second plane to be shared between data and control.

43. (New) The apparatus of claim 39 wherein the plurality of heterogeneous processing elements are configurable to communicate over the plurality of mesh interconnect networks using packets of information.

44. (New) An apparatus including a medium to hold machine-accessible instructions that when accessed result in a machine performing:

translating a design description into a configuration for a plurality of heterogeneous processing elements in a heterogeneous reconfigurable device coupled to routers interconnected by a plurality of mesh interconnect networks, the plurality of mesh interconnect networks being allocatable to either data or control or a combination thereof;

allocating the plurality of mesh interconnect networks between data and control, wherein translating and allocating results in a protocol file;

storing the protocol file in a memory; and

translating a second design description and performing a second allocation, resulting in a second protocol file, and storing the second protocol file in the memory.

45. (New) The apparatus of claim 44 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises dedicating the first plane to control and dedicating the second plane to data.

46. (New) The apparatus of claim 44 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises allocating the first plane to be shared between data and control.

47. (New) The apparatus of claim 44 wherein the plurality of mesh interconnect networks includes a first plane and a second plane, and allocating comprises allocating both the first plane and the second plane to be shared between data and control.

48. (New) The apparatus of claim 44 wherein the plurality of heterogeneous processing elements are configurable to communicate over the plurality of mesh interconnect networks using packets of information.